Our Docket No.: 42P16890

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Stone

Application No.: 10/666,462

Filed: September 19, 2003

For: Integrated Circuit Package with a Varied Pitch Distance

Examiner: Hyeon, Hae M.

Art Group: 2839

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 CFR 1.131 IN SUPPORT OF PRIOR INVENTION

Sir :

We, Brent Stone, Kenneth Kassa, Brian DeFord and Erik Peter declare:

1. We are the inventors of the claims of the above-captioned patent application ("the Application") and are the inventors of the subject matter described therein.

2. Prior to March 31, 2003, the filing date of U.S. Patent No. 6,752,635 cited in a Final Office Action mailed October 26, 2005, the invention claimed in the Application had been conceived and reduced to practice in the United States.

3. Attached Exhibit A is a redacted copy of an invention disclosure form describing the design of the Integrated Circuit Package with a Varied Pitch Distance, and

establishes that the subject matter claimed in the Application had been conceived and reduced to practice in the United States prior to March 31, 2003.

We further declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application of any patent issuing thereon.

Dated: 2/24/, 2006 _____
Brent Stone

Dated: _____, 2006 _____
Kenneth Kassa

Dated: _____, 2006 _____
Brian DeFord

Dated: _____, 2006 _____
Erik Peter

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Dated: _____, 2006

Brent Stone

Dated: _____, 2006

Kenneth Kassa

Dated: FEB 23, 2006

Brian DeFord

Dated: _____, 2006

Erik Peter

ATTN: LEAH Schwenke

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Dated: _____, 2006 _____
Brent Stone

Dated: _____, 2006 _____
Kenneth Kassa

Dated: _____, 2006 _____
Brian DeFord

Dated: FEB 23RD, 2006 _____
Erik Peter

5. **HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM (use first inventor's supervisor if multiple inventors)**

   DATE: _____ **SUPERVISOR NAME:** _____

   BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID.

6. **Has subject matter of present disclosure been disclosed or will it be disclosed outside Intel?**
   If yes, explain and give date: *Yes. This concept is incorporated in socket/package development for 1262 product and will be disclosed to socket suppliers by ww30'02.*
   (Give expected tape out date if applicable): *Prescott-T PTQ Q1'04*

7. **Has the subject matter of present disclosure been published or will it be published outside of Intel?**
   If yes, explain and give date: *Yes, this information will be released to strategic socket suppliers under NDA in Q3'03. It will be included in Intel's official design socket and package design specifications to be publicly released in 2004.*

8. **Has a product using or manufactured using the present disclosure been sold or offered for sale?**
   If yes, explain and give date: *Prototype mixed pitch stamped contact LGA sockets were received from strategic socket suppliers as part of an initial feasibility study were created for proof of concept.*

9. **Has this invention been conceived, or constructed during accomplishment of a government or third party contract? If yes, give contract name and number:** *No*

10. **Explain the problem being addressed by the invention:**

    This invention addresses the problem of: *increasing I/O and power delivery interconnect performance is resulting in high pin count devices that adversely affect motherboard, socket, and package costs. Increasing package size, decreasing motherboard routing trace widths, and pitch reduction on the socket all may result in increasing component costs due to increased manufacturing capability requirements. Additionally increases in package size negatively impact placement of components around the package on the motherboard. A mixed pitch stamped contact LGA and Package provides an optimum solution to address this problem.*

11. **Explain current state of the art (i.e, how the problem is solved today):**

    Presently the problem described above is solved by:
    Increased contact count is currently addressed by maintaining a uniform contact pitch and uniformly reducing pitch and/or increasing the package size. Either motherboard capability increases or package size increases are required, with respective cost and motherboard real estate increases per option.

12. **Explain technical advantages of the invention over current state of the art:**

    The technical advantage of this invention is:

    The contact density of the interconnect can be increased without requiring improved motherboard routing and socket manufacturing capabilities. The resulting increase in contact density allows for a smaller package, smaller socket, and a corresponding reduction in motherboard real estate; all allow for cost optimized components to be created without sacrificing performance.

EXHIBIT A

13. a. **Is the invention experimentally verified?** *Yes. Land Grid Array sockets with 735 contacts and a mixed pitch of 43 mils by 50 mils were manufactured and tested.*

    b. **Is the invention verified with simulation?** *Yes. Motherboard routing studies and package and motherboard capability studies have been performed.*

    c. **If neither a. or b. above, then you can get a patent on the concept, but please explain the technical basis to justify that your invention will work (use extra space if necessary):**

14. Detailed Description of Invention (try to use only the space provided with font #10 or larger type. Refer to your drawings):

Prior to this invention, the only ways to increase socket land count were to grow body size (with uniform, fixed pitch) and/or to reduce pitch (with same uniform, fixed pitch). Figures 1a and 1b depict a fixed pitch interconnect package viewed on the interconnect side. There is also a practical high volume manufacturing (HVM) limit on how far socket land pitch can be reduced. At this time something larger than 1mm in any dimension represents that HVM limit for stamped metal contact land grid array (LGA) sockets. Therefore, if a target land count cannot be reached given a desired body size and the minimum HVM pitch limit, then the only way to increase land count is to grow body size over the target. Growth to CPU body size represents significant cost to Intel and our customers because all components of the total CPU solution increase in cost.

The next key boundary condition for footprint (land position within a body size) definition has to do with the motherboard routing technologies to be used in breaking out the signals from the socket. At this time, it is generally agreed that a 5mil line width and 5mil line-2-line space paired with a 25mil pad VIA and an 18mil socket pad represent the industry standard technology base for motherboard routing rules (Figures 2 and 3). The combination of these technologies with the desired Signal-to-GND ratio for the device will limit how many rows deep land side motherboard breakout can go (see Figures 4 & 6). Non-land side breakout on the motherboard is limited by line geometries, via pad size, and via pitch (see Fig 6).

When used with stamped metal Land Grid Array Socket contacts, there is a constraint on minimum pitch in at least one axis introduced by the current stamped metal contact LGA designs, which extends horizontally away from true center of each pad location. Figure 8 depicts a cross section of a LGA socket with stamped metal contacts; reduction of the contact pitch in the "Y" direction is limited by required deflection in the stamped contact beam, however the "X" dimension (into the plane of the picture) can be reduced. Figure 9 depicts a top view of an evaluated mixed pitch implementation with X=46mis, Y=50mils. The outlined boxes in figure 1b depicts how groups (gangs) of LGA stamped metal contacts are typically inserted into a socket housing and demonstrates how the mixed pitch socket can leverage current manufacturing technology. The actual pitch in both "X" and "Y" dimensions of the footprint are tailored to work with these motherboard technology and contact design limitations (see Figs 1-x).

As motherboard technologies and contact design constraints advance, future component footprints can utilize the same method for optimizing total number of lands and directional pitch.

15. Drawings (use as many pages as needed)

Figure 1. Present State of the Art: Fixed Pitch Interconnect (X=Y)
(a) View from bottom side of package.
(b) Motherboard view

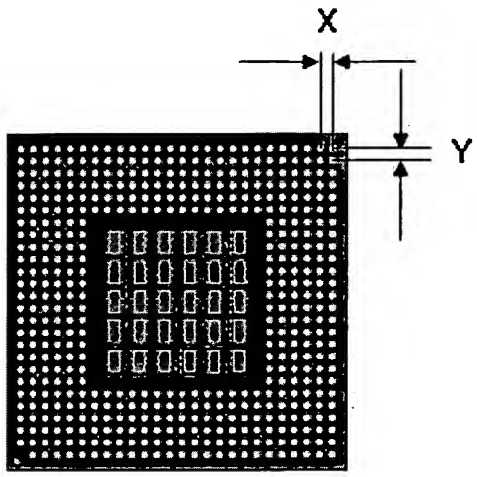


Figure 1a.

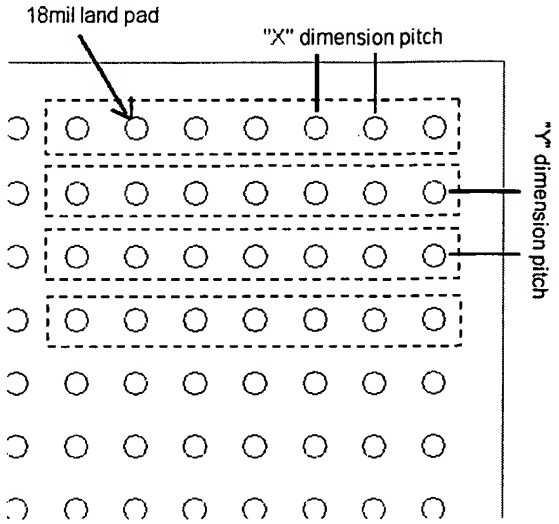
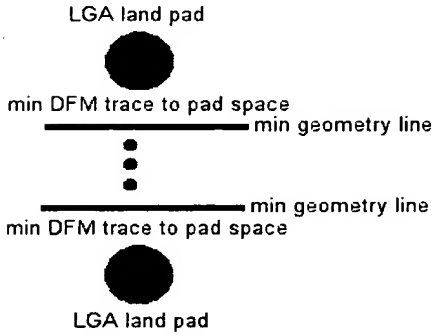
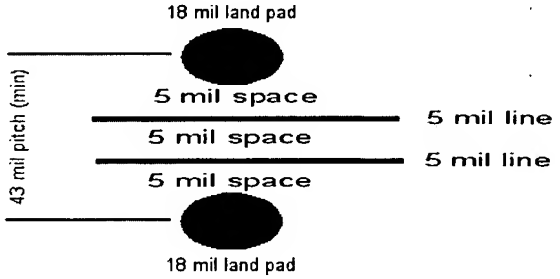


Figure 1b.

Figure 2. Defining Pitch to Meet Motherboard Route Technology Baselines (Component Side Escape)



Generic Limit



Current PCB technology Limit

Figure 3 – Defining Pitch to Meet Motherboard Route Technology Baselines (Non-Component Side Escape)

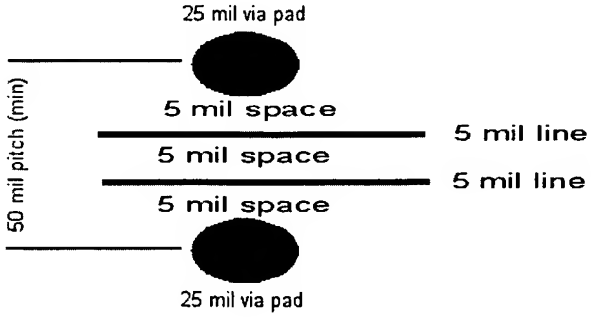


Figure 4 – Motherboard Breakout Depth Constraint (Land Side)

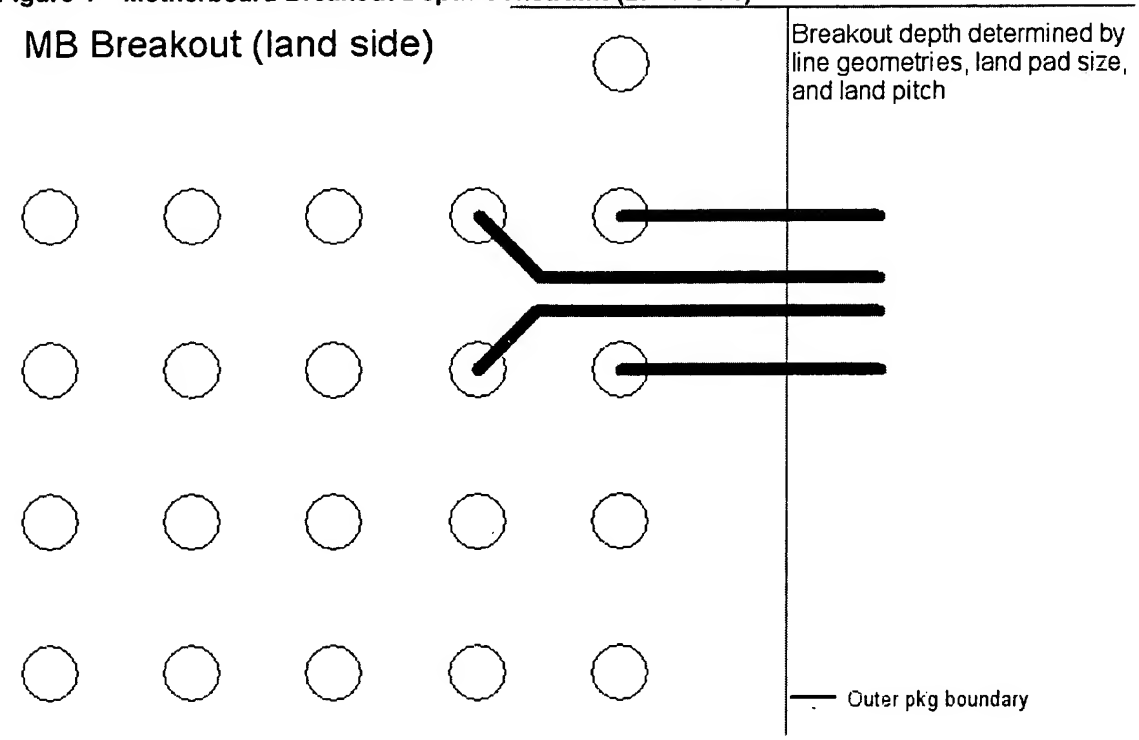


Figure 5 – Sample Footprint with Uniform, Mixed Pitch

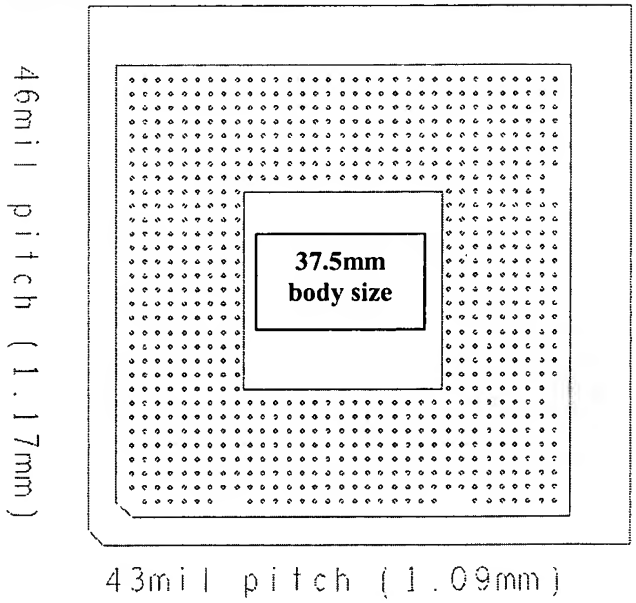


Figure 6 – Actual Motherboard Breakout for Uniform, Mixed Pitch LGA Sockets Using Industry Standard PCB Technologies

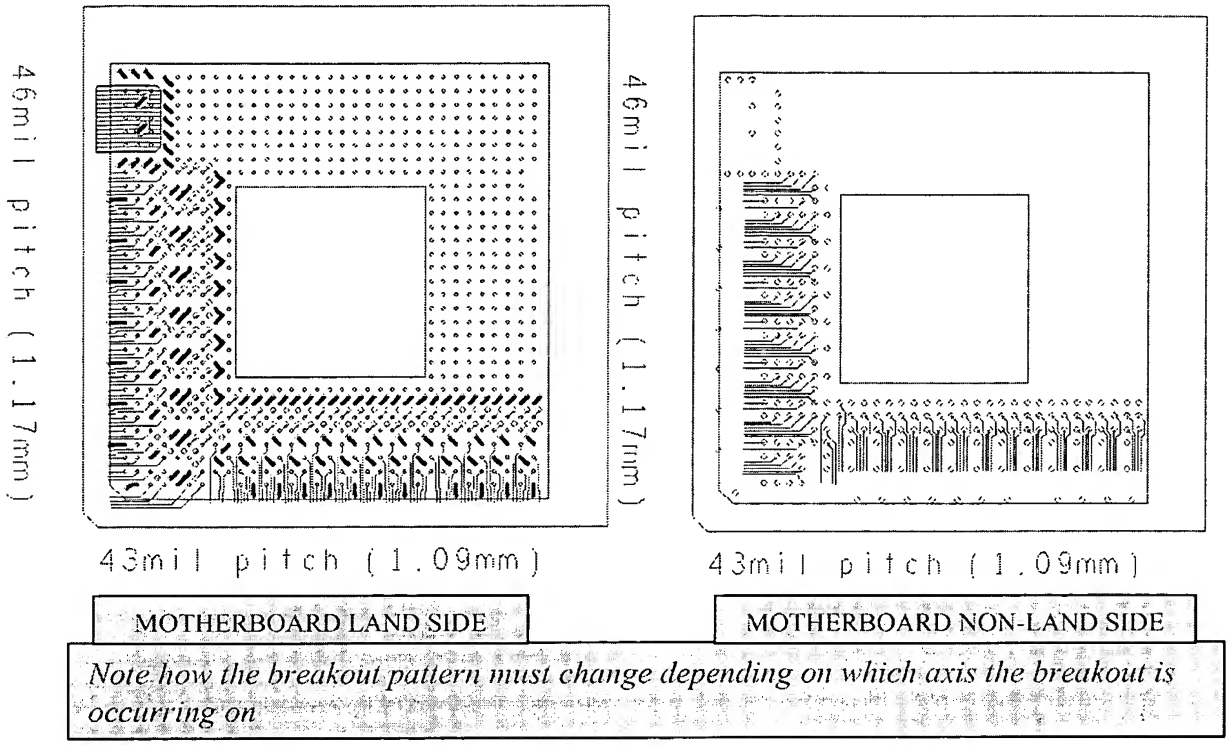


Figure 7- Embodiment of the Invention: Mixed pitch interconnect

(a) View from bottom side of mixed pitch LGA package, x=1.09mm, y=1.27mm

(b) Isometric view of corresponding mixed pitch LGA socket, x=1.09mm, y=1.27mm

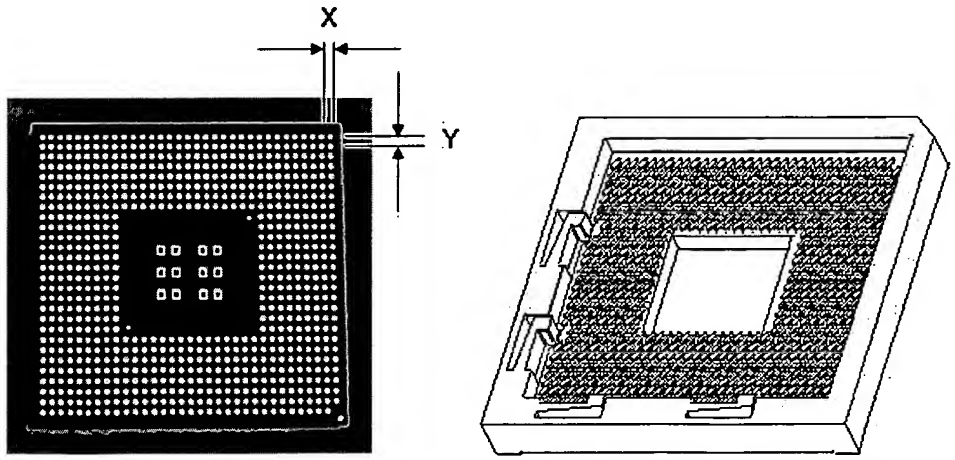


Figure 8- Cross section of electronic package with stamped metal contact LGA socket

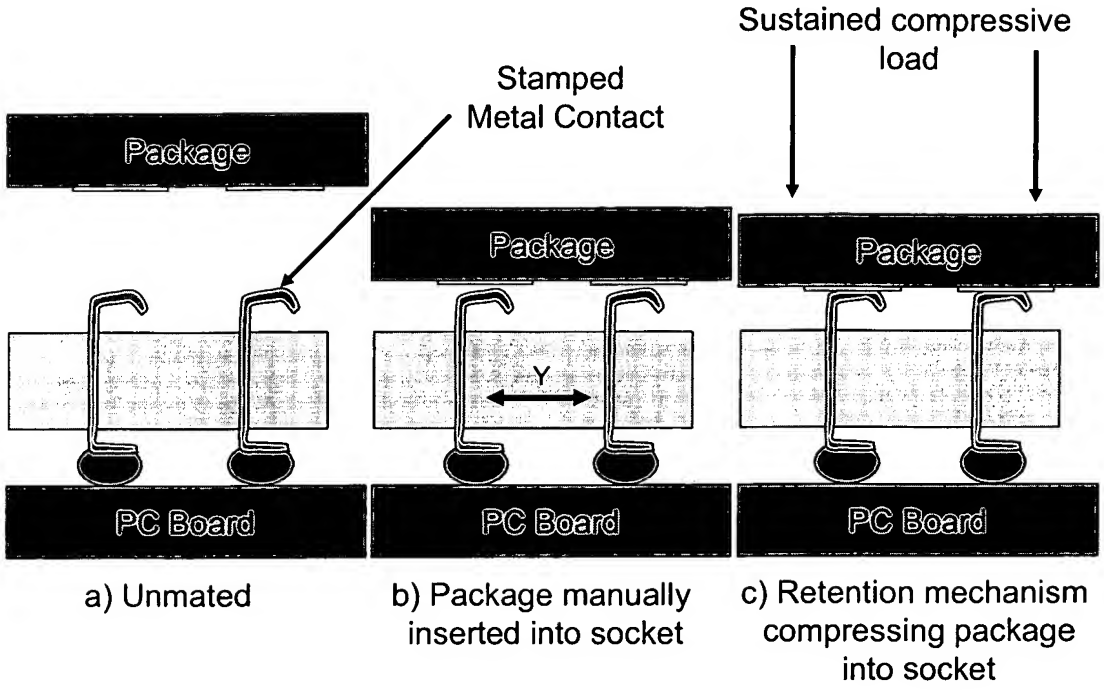
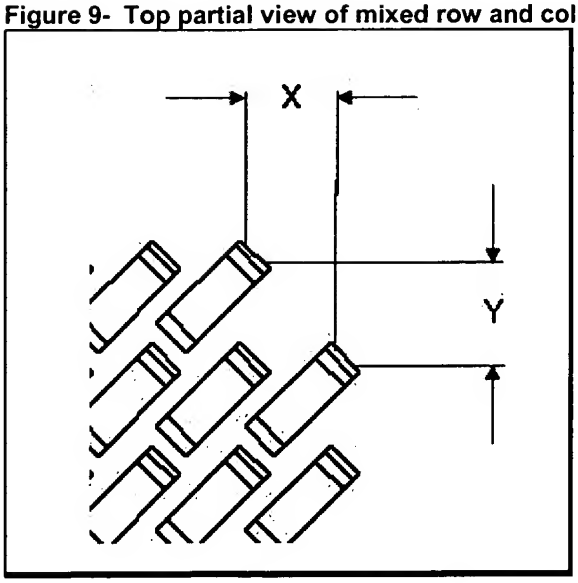


Figure 9- Top partial view of mixed row and columnar pitch stamped contact LGA socket



16. **Key Supporting Data (1 page limit on separate page):**

Figures 7A and 7B show a package and socket design to use a mixed pitch interconnect of 1.09mm x 1.27mm. Sockets were also prototyped and function with mixed pitch packages. Figure 6 depicts a motherboard routing study performed to confirm the validity of the board routing claim.

17. **What is the product or process invention to be used on? (e.g., P8xx, name of product, etc.):**
Prescott-T, Tejas 1262 product (all Socket T products and technology extensions)

18. **Have you reviewed your invention with a TMG Patent Mentor? (see below for mentor names) If so, give name: _____No__X_____**